

AT91RM9200-EK Evaluation Board

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User Guide





Table of Contents

Section 1

Overview	1-1
1.1 Scope	1-1
1.2 Deliverables	1-2
1.3 The AT91RM9200-EK Evaluation Board	1-3

Section 2

Setting Up the AT91RM9200-EK Evaluation Board	2-1
2.1 Electrostatic Warning	2-1
2.2 Requirements	2-1
2.3 Powering Up the Board	2-1
2.4 Getting Started with the AT91RM9200	2-1

Section 3

Board Description	3-1
3.1 AT91RM9200 Processor	3-1
3.2 Memory	3-2
3.3 Memory Card	3-2
3.4 Clock Circuitry and Analog Functions	3-2
3.5 Reset Circuitry	3-2
3.6 Power Supply Circuitry	3-2
3.7 Remote Communication	3-2
3.8 User Interface	3-2
3.9 Expansion Slot	3-3
3.10 Debug Interface	3-3
3.11 Wrapping User Area	3-3

Section 4

Configuration Straps	4-1
4.1 Configuration Straps and Jumper Settings	4-1

Section 5

Schematics	5-1
5.1 Schematics	5-1



Section 1

Overview

1.1 Scope

The AT91RM9200-EK Evaluation Board enables real-time code development and evaluation. It supports the AT91RM9200 ARM9™-based 32-bit RISC microcontroller.

This guide focuses on the AT91RM9200-EK Evaluation Board as an evaluation and demonstration platform:

- Section 1 is this overview.
- Section 2 gives information on setting up the installation.
- Section 3 contains a description of the development board.
- Section 4 details the configuration straps.
- Section 5 shows board schematics.

1.2 Deliverables

The development kit is delivered with:

- One AC adapter 100 - 240V ~ 1.2A, 12V, 50 - 60 Hz with adapters
 - One modem RS232 cable
 - One RJ45 Ethernet crossed cable
 - One A/B-type USB cable
 - One AT91 DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.
 - CD ROMs from third parties, providing solutions for operating system evaluation
 - DataFlash® Cards to provide demonstrations of operating systems when inserted in the bootable slot
- Note:** To boot on a DataFlash Card:
- Ensure J15 (BMS) is set on position 1-2
 - Insert the DataFlash Card in the J200 socket (bottom side)
 - Reset the board

Further details are given on the AT91 DVD-ROM.

Note: These deliverables are subject to change without notice.

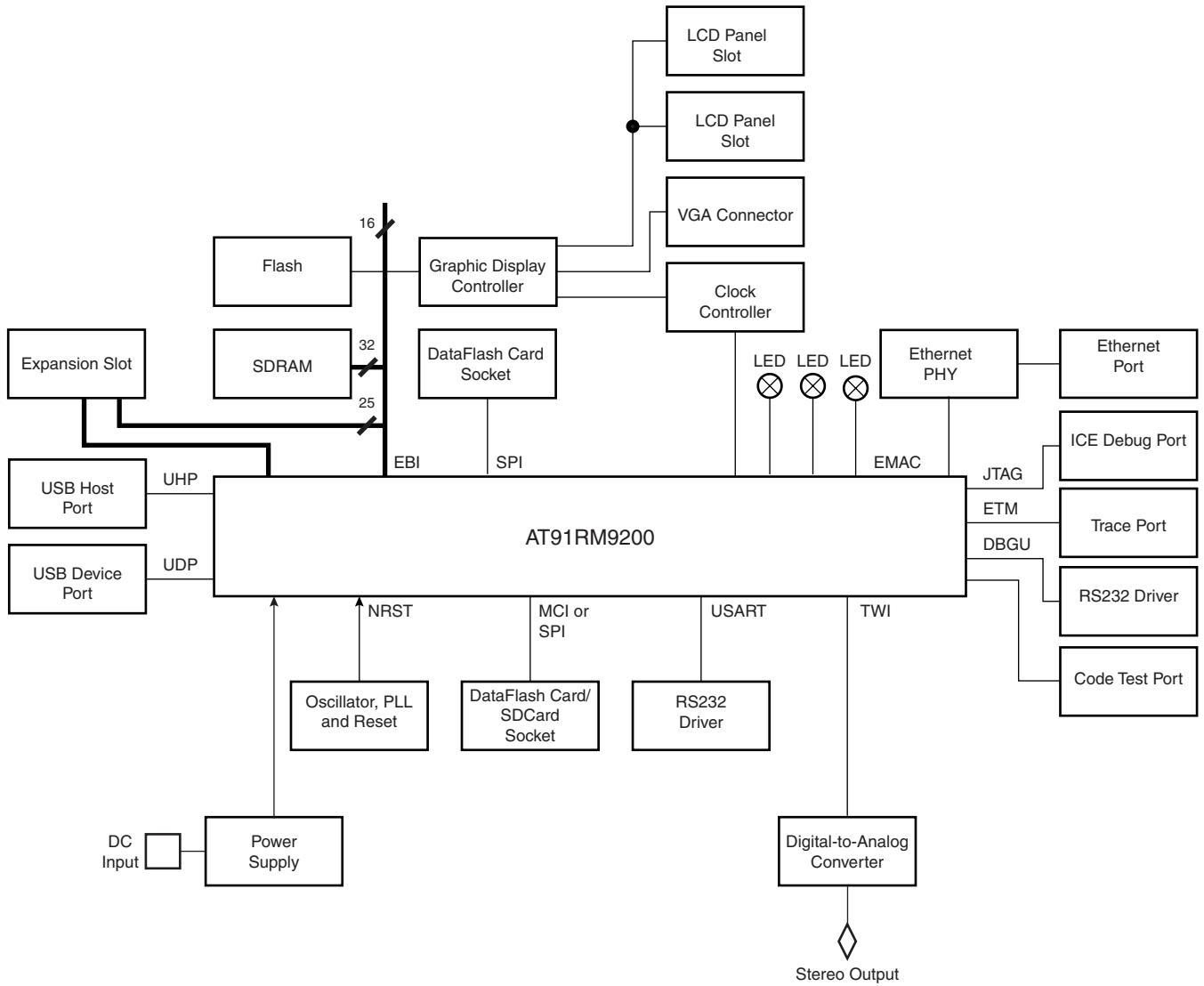
1.3

**The
AT91RM9200-EK
Evaluation Board**

The board consists of an AT91RM9200 together with the following:

- 8 Mbytes of parallel Flash memory
- Four banks of 2M x 32-bit SDRAM
- DataFlash[®] or SD/MMC memory expansion socket
- Additional DataFlash memory expansion socket
- Digital-to-Analog Converter (DAC) for a stereo audio signal
- Four communication ports (USB host and device, Ethernet, serial and DBGU)
- Graphic controller with output to a standard VGA monitor
- JTAG/ICE, ETM and code test port interface
- Expansion connector
- Onboard prototype area

Figure 1-1. AT91RM9200-EK Evaluation Board Block Diagram





Section 2

Setting Up the AT91RM9200-EK Evaluation Board

-
- | | | |
|------------|--|--|
| 2.1 | Electrostatic Warning | The AT91RM9200-EK Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element. |
| <hr/> | | |
| 2.2 | Requirements | <p>In order to connect the AT91RM9200-EK Evaluation Board, the following element is required:</p> <ul style="list-style-type: none">■ The AT91RM9200-EK Evaluation Board itself |
| <hr/> | | |
| 2.3 | Powering Up the Board | <p>DC power is supplied to the board via the 2.1 mm socket (J1). The polarity of the power supply is not critical. The minimum voltage required is 7V.</p> <p>The board has a voltage regulator providing +3.3V. The regulator allows the input voltage range to be from 7V to 12V.</p> |
| <hr/> | | |
| 2.4 | Getting Started with the AT91RM9200 | The AT91RM9200-EK Evaluation Board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/ , for the most up-to-date information on getting started with the AT91RM9200. |





Section 3

Board Description

- 3.1 AT91RM9200 Processor**
- Incorporates the ARM920T™ ARM® Thumb® Processor
 - 200 MIPS at 180 MHz
 - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
 - Memory Management Unit
 - In-circuit Emulator including Debug Communication Channel
 - Mid-level Implementation Embedded Trace Macrocell
 - Additional Embedded Memories
 - 16K Bytes of SRAM and 128K Bytes of ROM
 - External Bus Interface (EBI)
 - Supports SDRAM, Static Memory, Burst Flash, Glueless Connection to CompactFlash®, SmartMedia™ and NAND Flash
 - System Peripherals:
 - Enhanced Clock Generator and Power Management Controller
 - Two On-chip Oscillators with Two PLLs
 - Very Slow Clock Operating Mode and Software Power Optimization Capabilities
 - Four Programmable External Clock Signals
 - System Timer Including Periodic Interrupt, Watchdog and Second Counter
 - Real-time Clock with Alarm Interrupt
 - Debug Unit, Two-wire UART and Support for Debug Communication Channel
 - Advanced Interrupt Controller with 8-level Priority, Individually Maskable Vectored Interrupt Sources, Spurious Interrupt Protected
 - Seven External Interrupt Sources and One Fast Interrupt Source
 - Four 32-bit PIO Controllers with Up to 122 Programmable I/O Lines, Input Change Interrupt and Open-drain Capability on Each Line
 - 20-channel Peripheral DMA Controller (PDC)
 - Ethernet MAC 10/100 Base-T
 - USB 2.0 Full Speed (12 M-bits per second) Host Double Port and Device Port

- MultiMedia Card Interface (MCI)
- Three Synchronous Serial Controllers (SSC)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
- Master/Slave Serial Peripheral Interface (SPI)
- Two 3-channel, 16-bit Timer/Counters (TC)
- Two-wire Interface (TWI)
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins

-
- 3.2 Memory**
- 8-Mbyte parallel Flash memory
 - Four banks of 2M x 32-bit SDRAM

-
- 3.3 Memory Card**
- SD Card/MMC
 - Supports MultiMedia and SD Card
 - Analog switches provide support for DataFlash[®] Card
 - Additional DataFlash Card Socket

-
- 3.4 Clock Circuitry and Analog Functions**
- 32.768 kHz standard crystal for the AT91RM9200
 - 18.432 MHz standard crystal for the AT91RM9200
 - 50 MHz CMOS oscillator for the Display Controller and Ethernet PHY

-
- 3.5 Reset Circuitry**
- Reset Controller

-
- 3.6 Power Supply Circuitry**
- 3.3V DC/DC converter
 - 1.8V DC/DC converter

-
- 3.7 Remote Communication**
- Fast Ethernet Physical Layer Single Chip Transceiver
 - Host Interface via RS-232 DB9 male socket
 - Debug Port via RS-232 DB9 connector
 - Host and Device USB socket

-
- 3.8 User Interface**
- Graphic Display Controller
 - TFT/SNT panel socket
 - 15-pin standard socket for an external VGA monitor

- Three LEDs managed via general PIO lines
- Stereo Audio Jack connected to a DAC

3.9 Expansion Slot ■ The expansion slot gives access to all the microcontroller's signals.

3.10 Debug Interface

- 38-pin trace Port socket (ETM)
- 38-pin Code Test port socket
- 20-pin JTAG ICE interface connector
- Serial Debug Unit

3.11 Wrapping User Area ■ Onboard prototype area allowing the developer to fit additional components.





Section 4

Configuration Straps

4.1 Configuration Straps and Jumper Settings

Table 4-1 gives details on configuration straps and jumper settings on the AT91RM9200-EK Evaluation Board and their default settings.

Table 4-1. Configuration Straps and Jumper Settings

Designation	Default Setting	Feature
J13	Closed	Available for measuring VDDCORE current.
J15	1 - 2	The AT91RM9200 boots from internal ROM and can also boot from external SPI DataFlash [®] connected on NPCSO.
	2 - 3	The AT91RM9200 boots from Flash memory connected on NCS0.





Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- AT91RM9200-EK Board Layout - Top View
- AT91RM9200-EK Board Layout - Bottom View
- Power Supply
- AT91RM9200 Chip
- Debug
- SDRAM and Flash
- RMI Ethernet
- Stereo Audio DAC
- Serial Interfaces
- VGA Display
- Expansion Connector

Figure 5-1. AT91RM9200-EK Board Layout - Top View

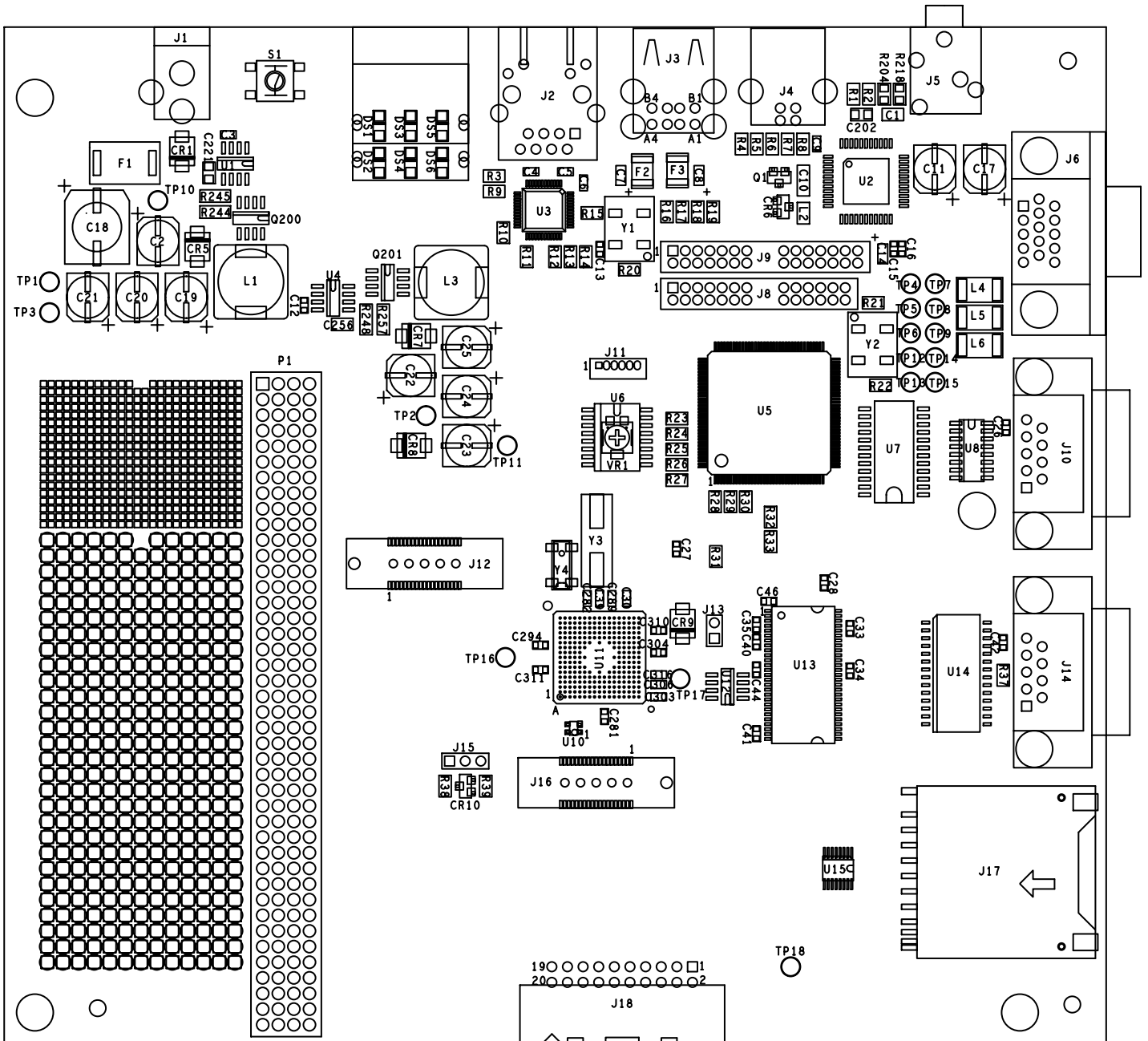
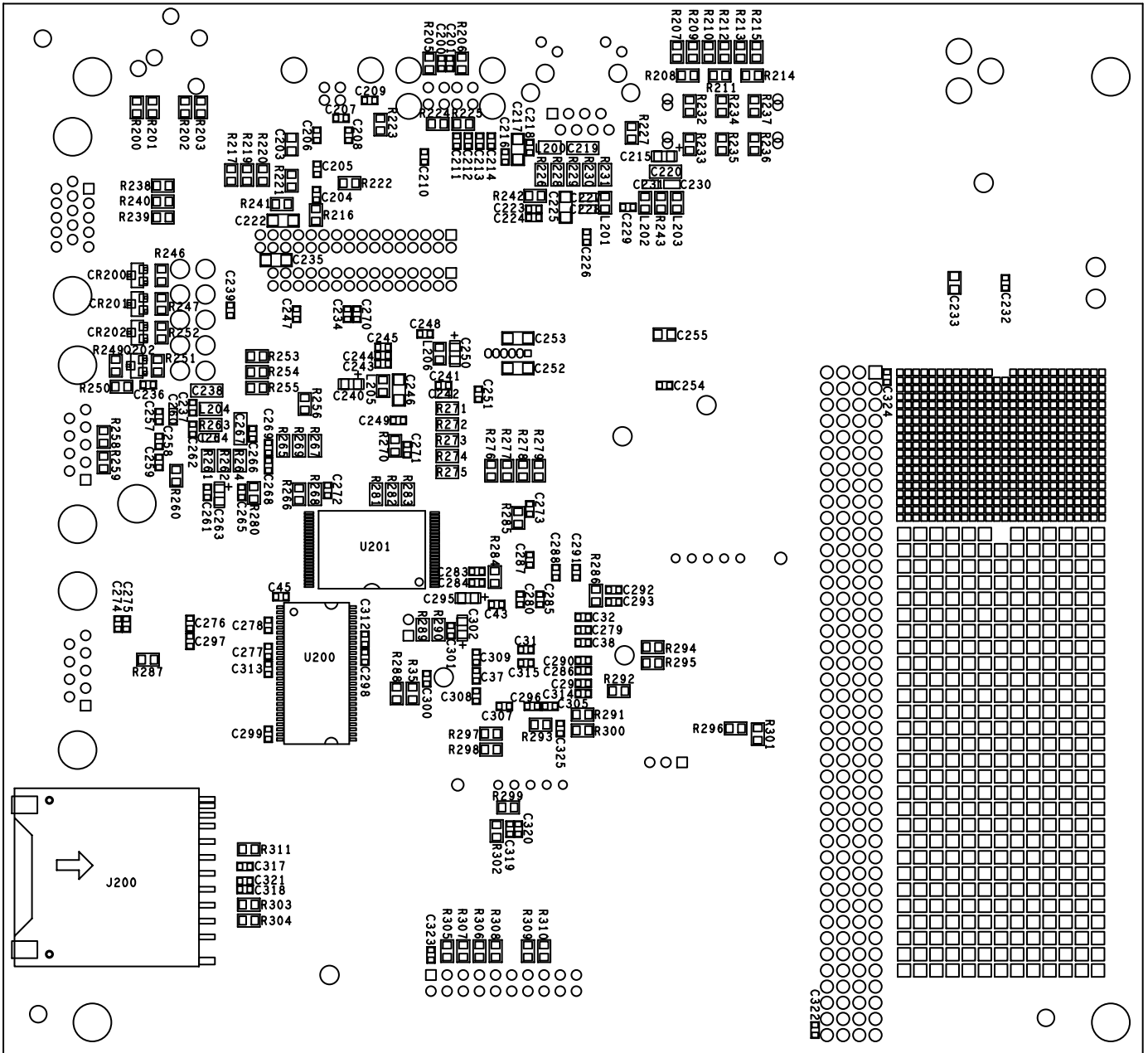
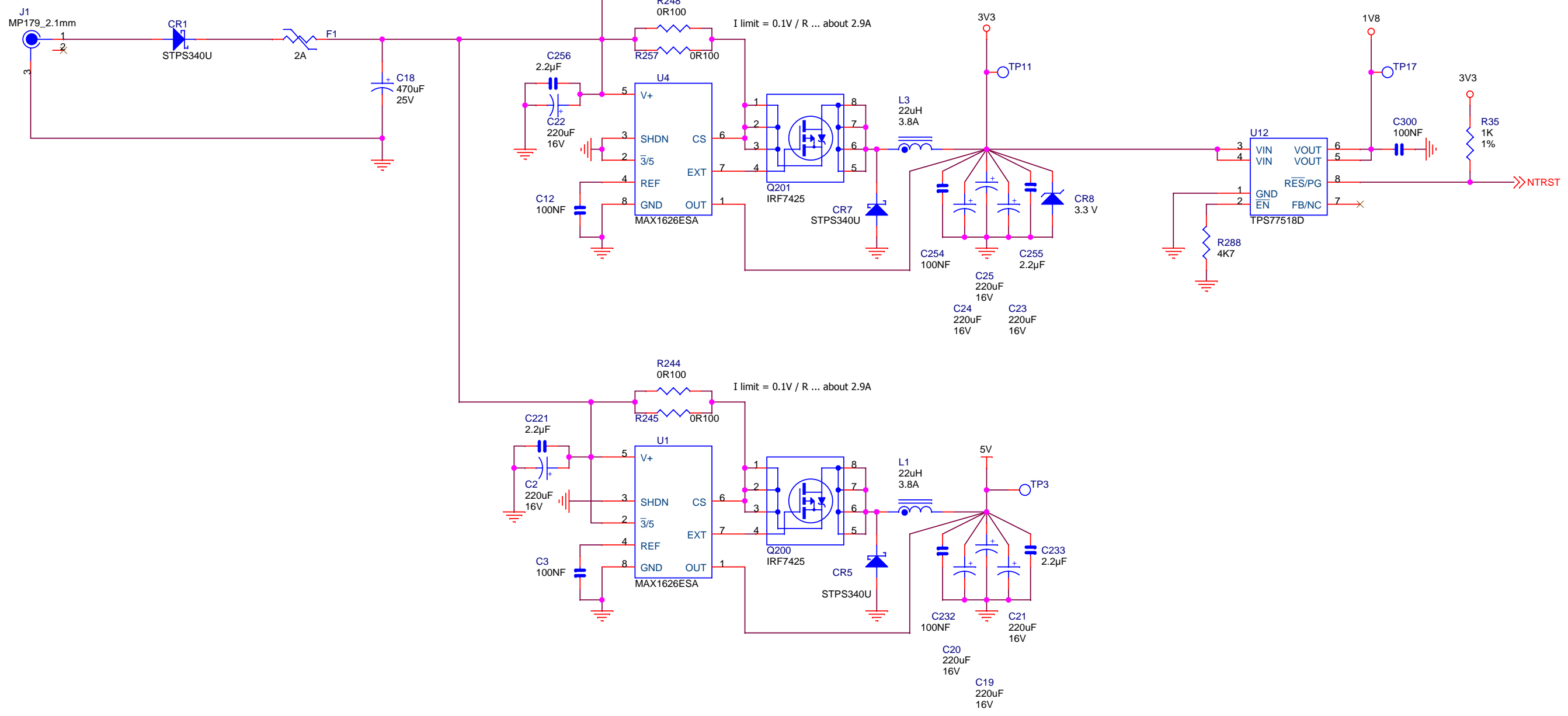


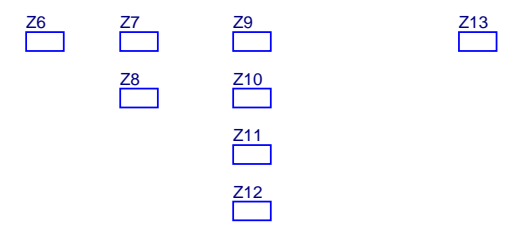
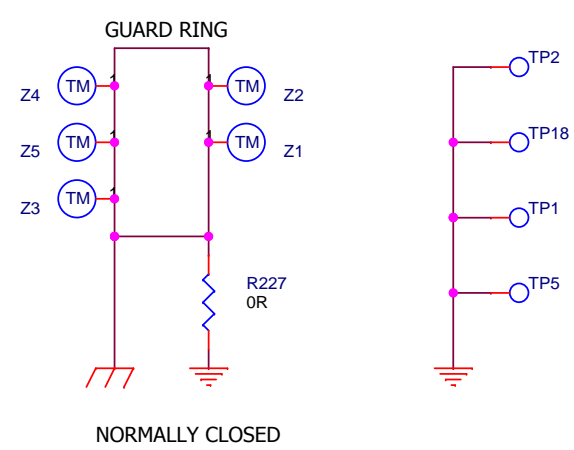
Figure 5-2. AT91RM9200-EK Board Layout - Bottom View



12V TO 14V DC INPUT



Z3 - Z5 are mounting holes.
The Z reference designators
are not listed on the actual
board.



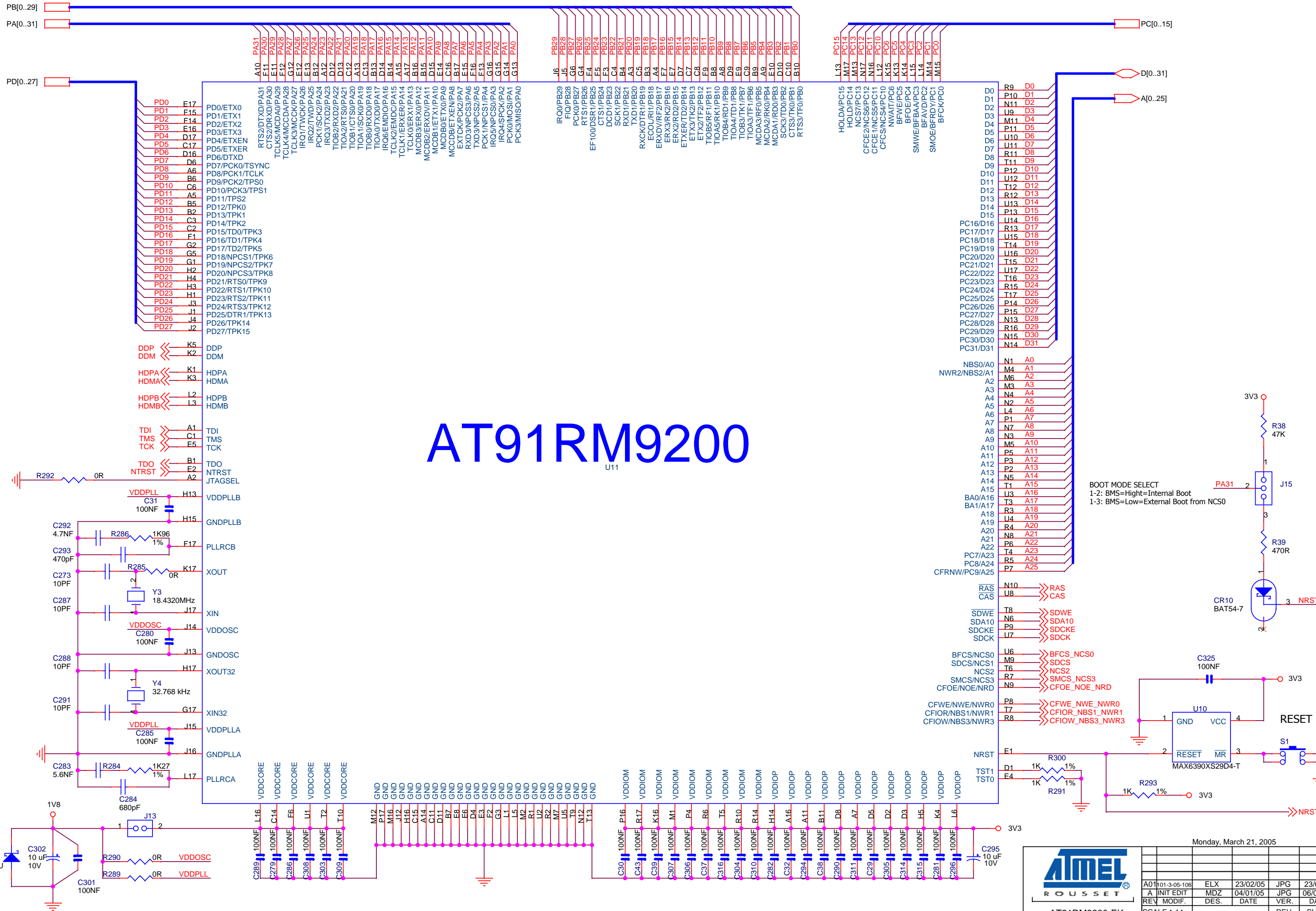
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AT91RM9200-EK		A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05
POWER SUPPLY		REV	MODIF.	DES.	DATE	VER.	DATE
SCALE 1/1		63SC042261A01		REV.	SHEET		1/9

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AT91RM9200

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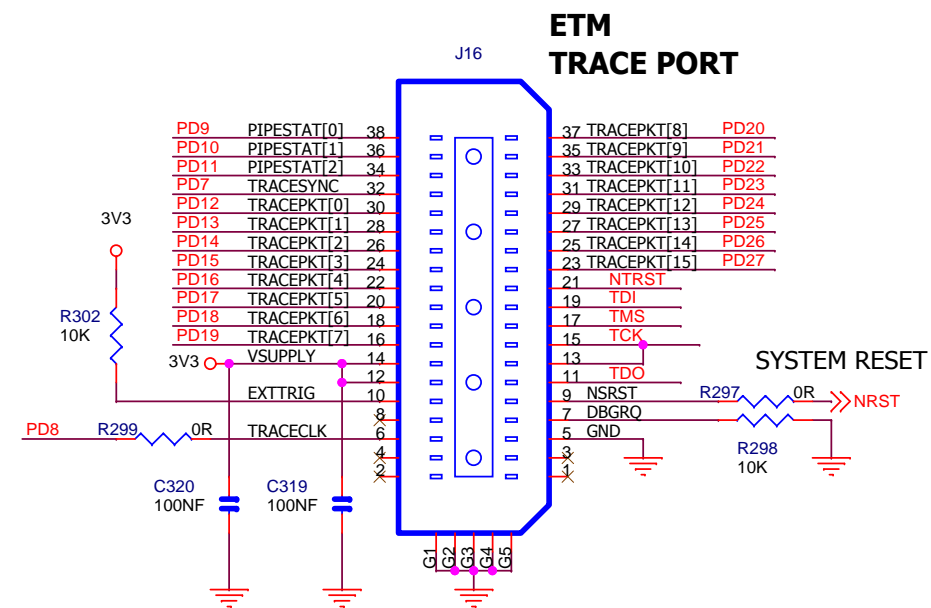
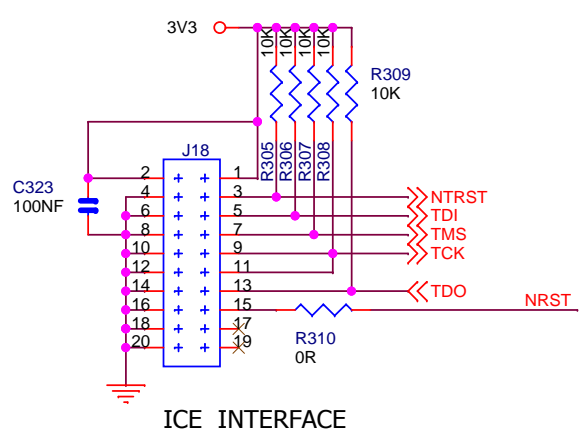
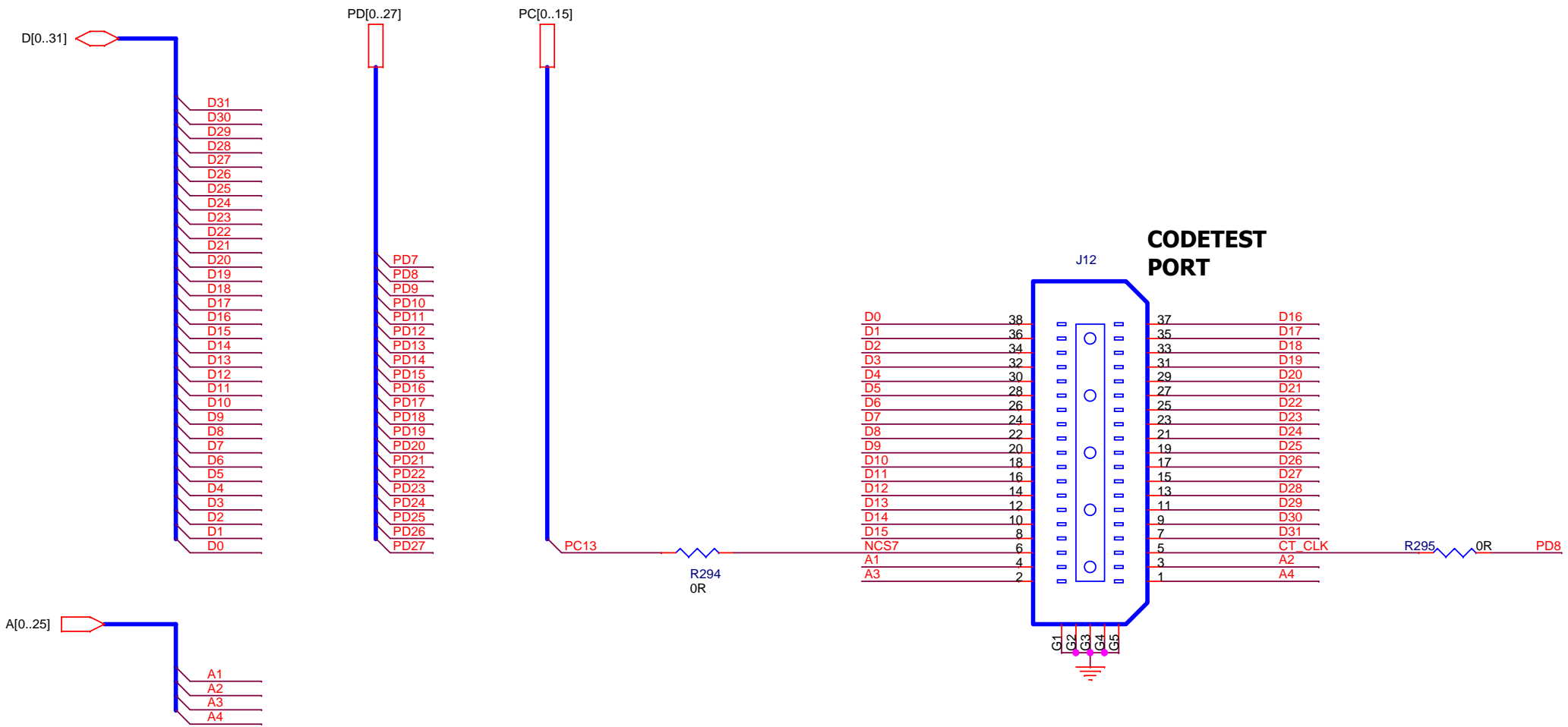


BOOT MODE SELECT
1-2: BMS=High=Internal Boot
1-3: BMS=Low=External Boot from NCS0

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A INIT EDIT	MDZ	04/01/05	JPG
REV	MODIF.	DES.	DATE
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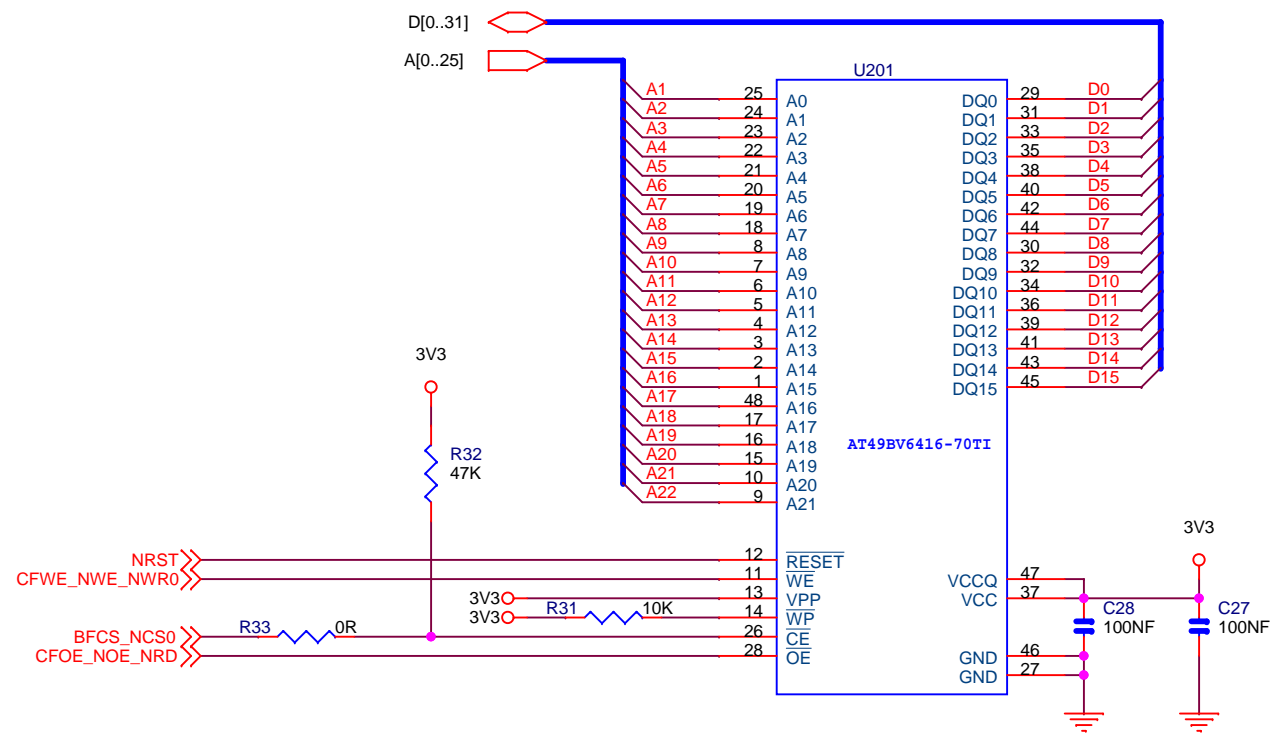
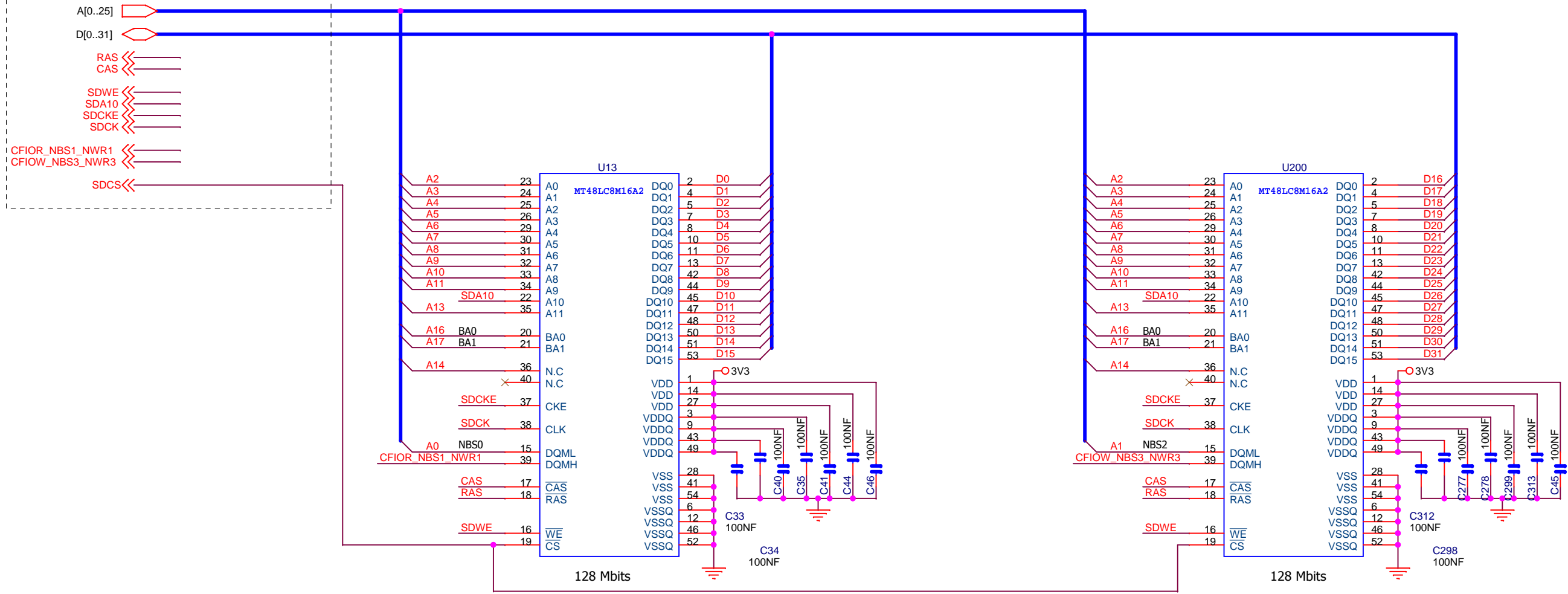


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ETM - ICE - TEST		SCALE	1/1	63SC04226		REV.	SHEET
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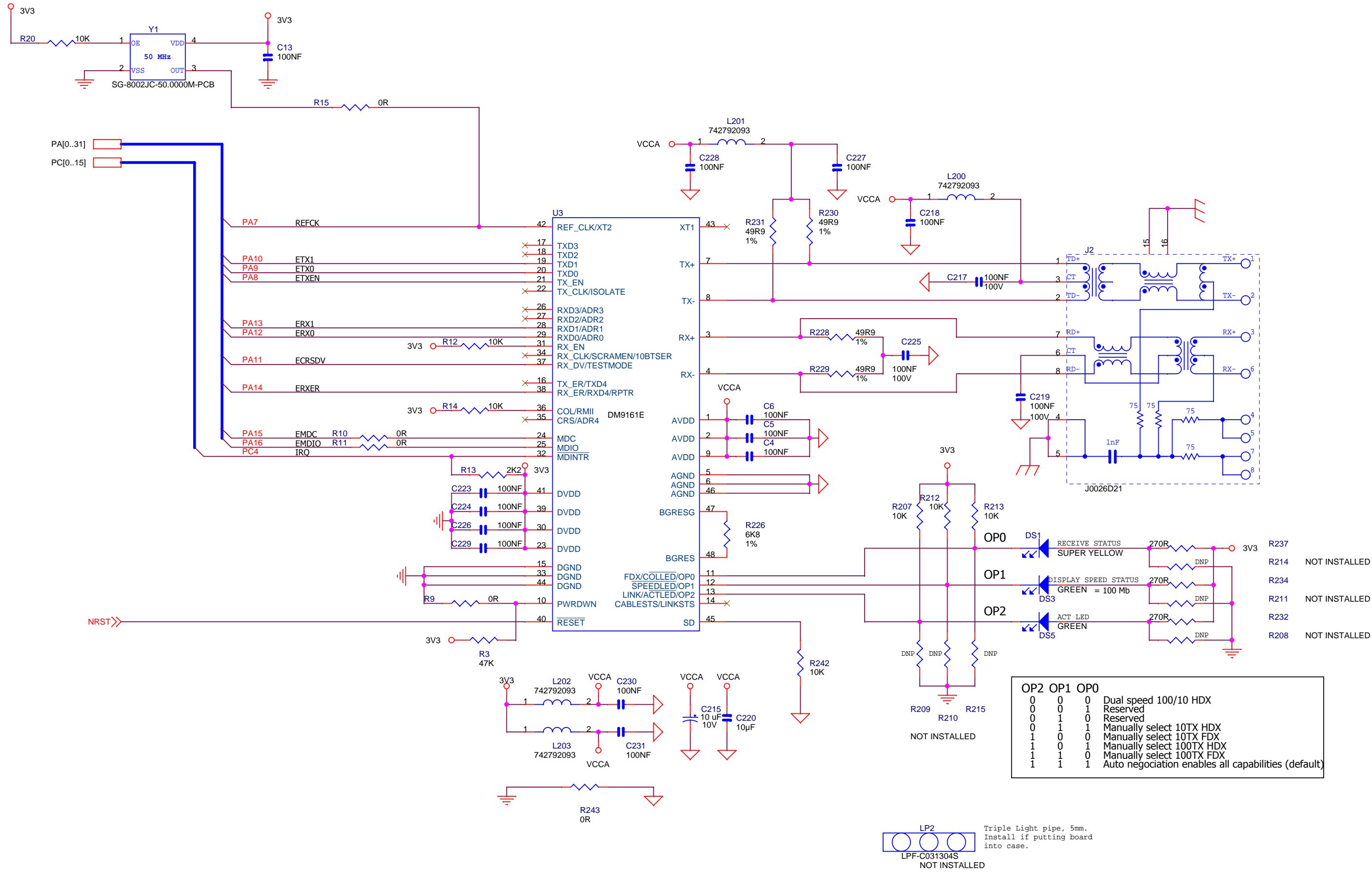
EBI SDRAM INTERFACE



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SDRAM & FLASH		63SC042261 A01		4/9	
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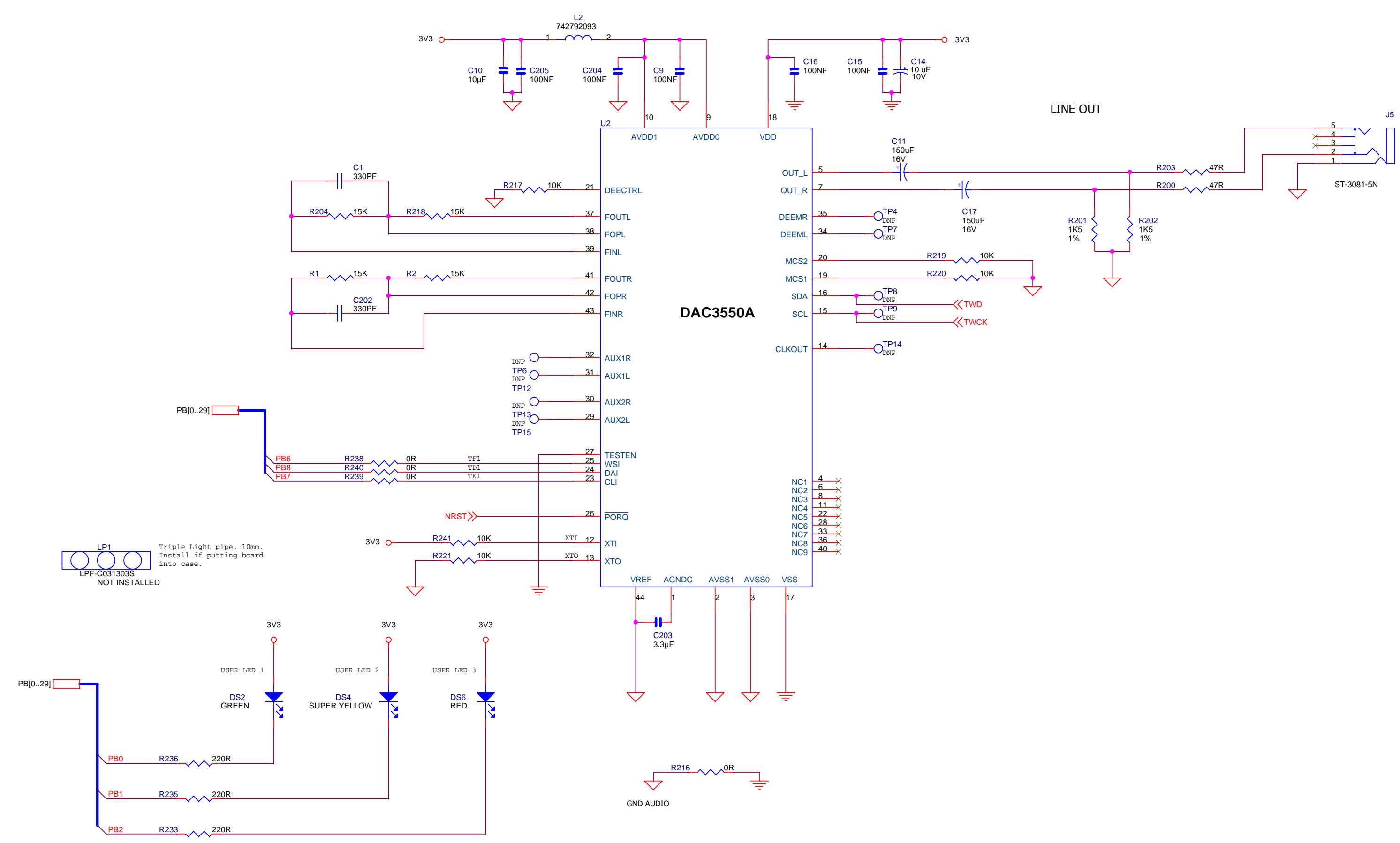


OP2	OP1	OP0	Description
0	0	0	Dual speed 100/10 HDX
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Manually select 10TX HDX
1	0	0	Manually select 10TX FDX
1	0	1	Manually select 100TX HDX
1	1	0	Manually select 100TX FDX
1	1	1	Auto negotiation enables all capabilities (default)

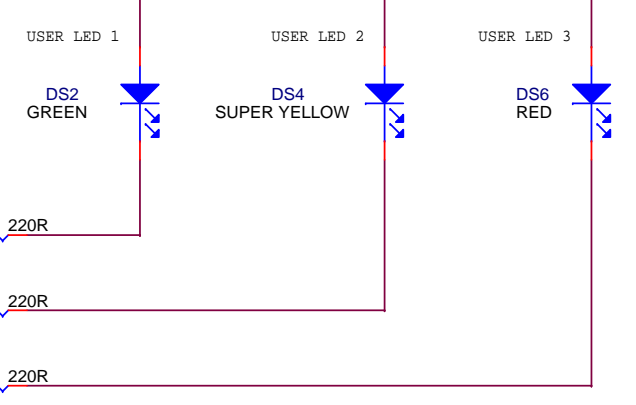
LP2 Triple Light pipe, 5mm.
Install if putting board into case.
LPF-C031304S NOT INSTALLED

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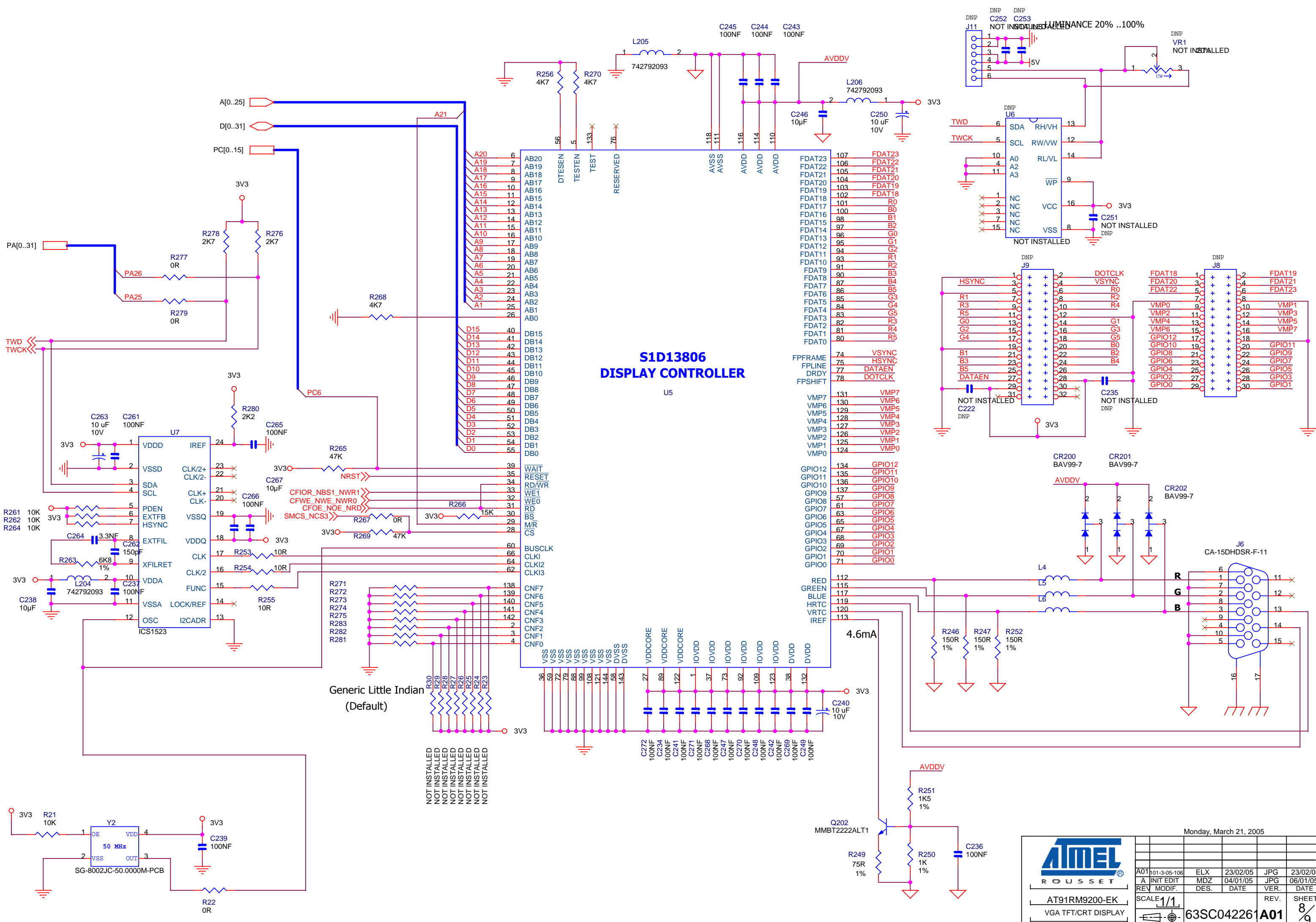
LP1 Triple Light pipe, 10mm.
Install if putting board into case.
LPF-C031303S
NOT INSTALLED



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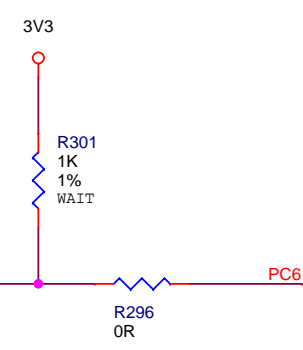
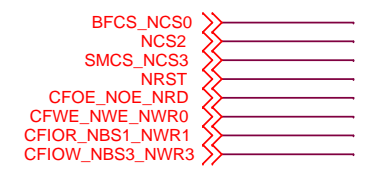
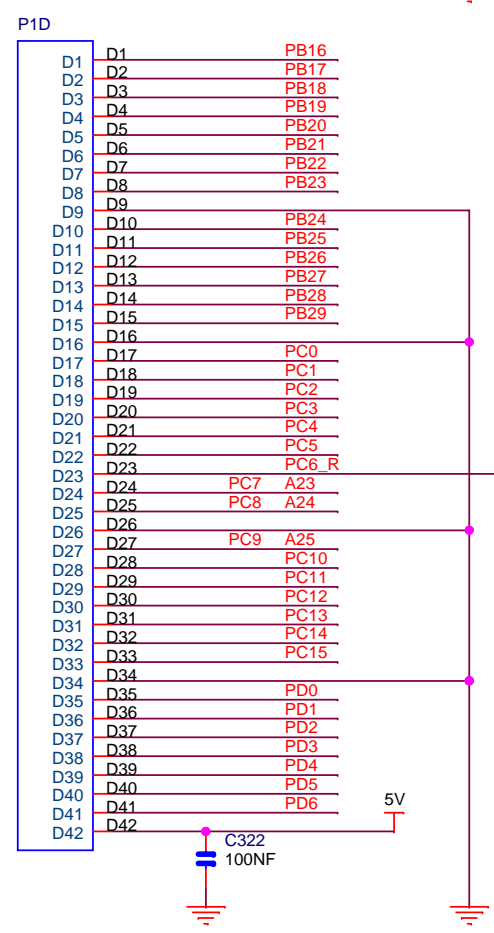
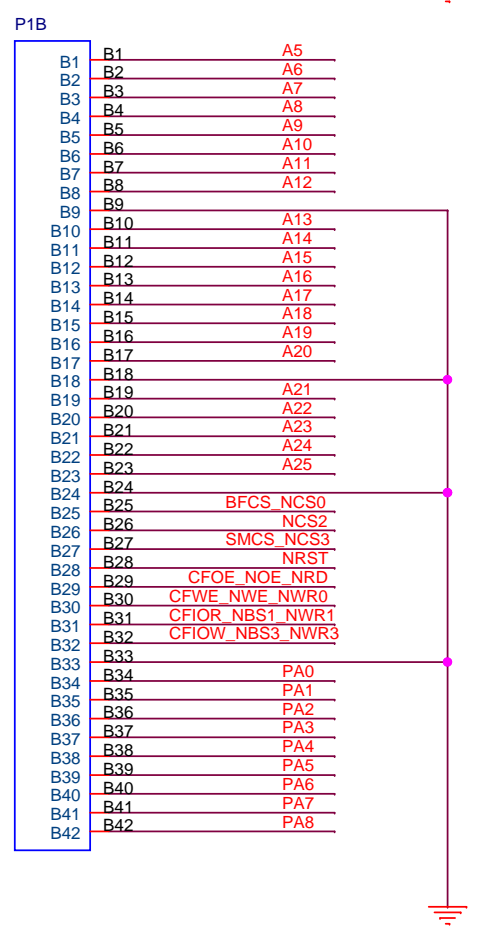
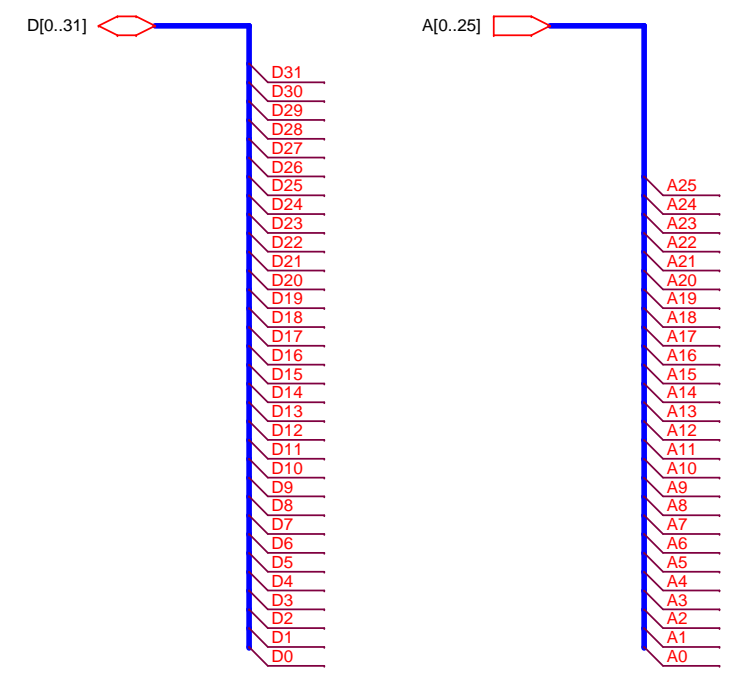
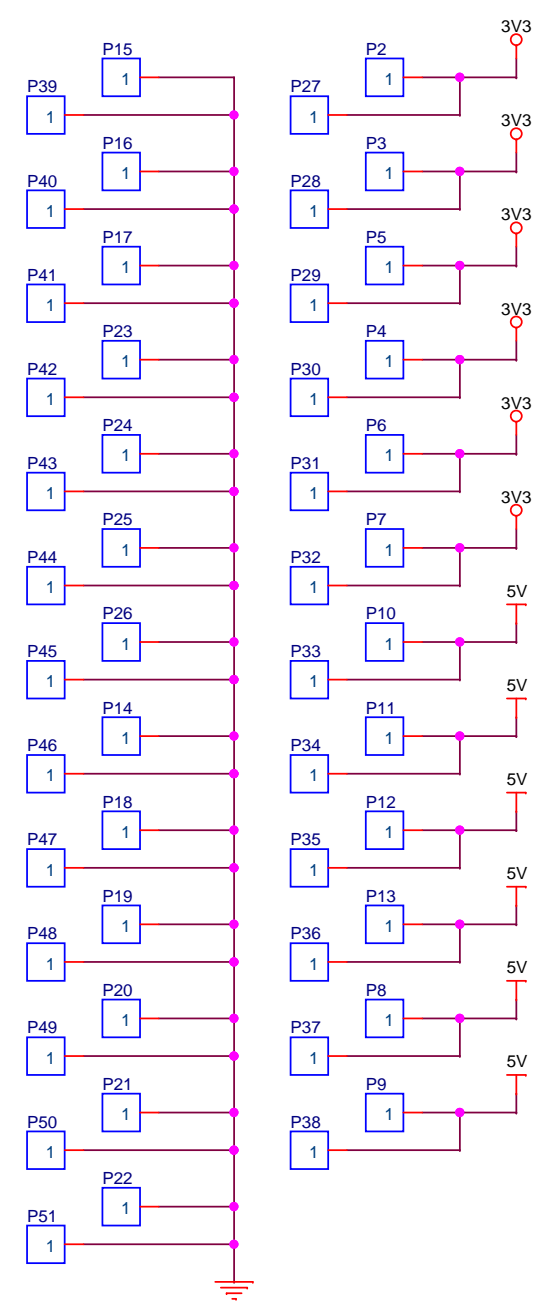
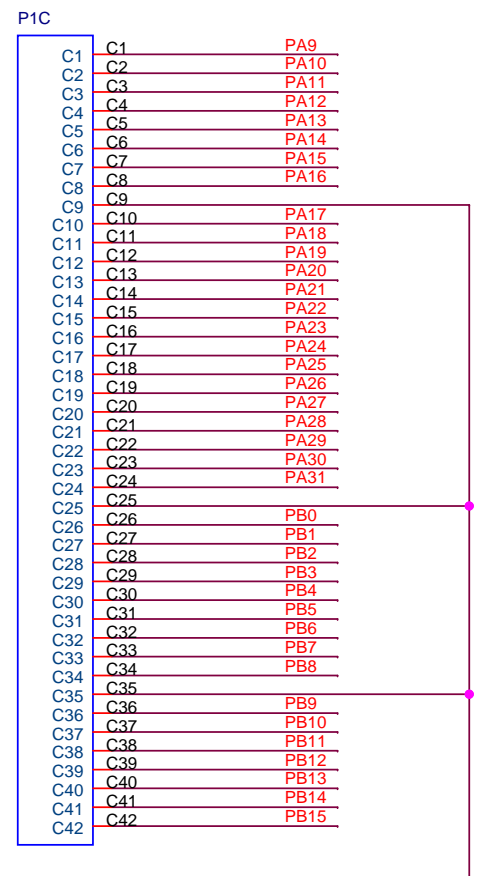
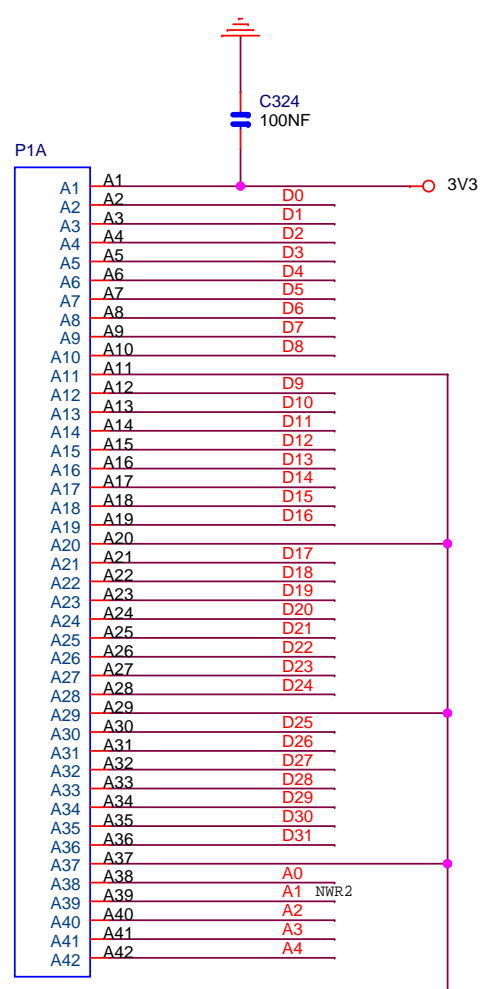
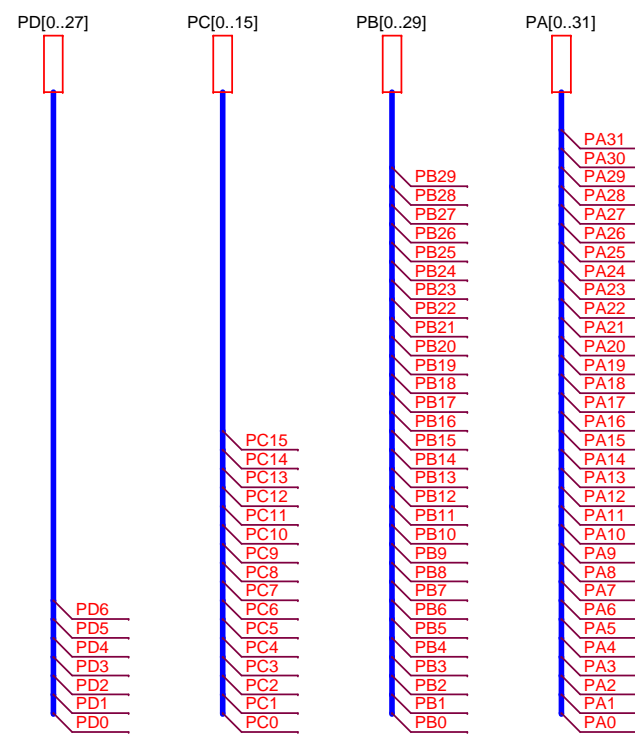


**S1D13806
DISPLAY CONTROLLER**

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AT91RM9200-EK
VGA TFT/CRT DISPLAY



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AT91RM9200-EK
EXPANSION CONNECTORS

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					9/9

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Revision History

Doc. Rev.	Date	Comments	Change Request Ref.
6103A	24-Sep-04	First issue.	
6103B	02-Mar-05 19-Jul-05	Section 1.2, "Deliverables" on page 2; List simplified Table 4-1, Boot information modified New schematics added in Section 5.	CSR 04-361, CSR 05-028, CSR 05-246



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